LivePlot_v12 build and installation

LivePlot works best on 32-bit or 64-bit Windows 7, or 32-bit Windows XP. It also runs on Windows 10, but a workaround is required.

Installation

Extract **LivePlot_v12.zip** to a new folder called **LivePlot_v12**

Downloading FFTW

Visit http://www.fftw.org/install/windows.html

Download either **fftw-3.3.5-dll32.zip**
or **fftw-3.3.5-dll64.zip**

Extract **libfftw3-3.dll** and place in subfolder **LivePlot_v12\fftw**

Xilinx JTAG drivers

LivePlot uses the Xilinx USB JTAG driver to control the SP605 board. Download and install either **Xilinx ISE 14.7** or **Xilinx Lab Tools 14.7**

Earlier Xilinx versions can be used; 13.3 and 14.7 have been tested; but 14.7 is the latest. Paths in the supplied files are configured for 14.7 and need editing to use an earlier version.

Xilinx have released a new version of 14.7 for Windows 10; but this installs the Linux version in a virtual machine and doesn't include the cable driver required by LivePlot.

Compiling LivePlot

LivePlot has been built successfully with Microsoft Visual Studio 6, Microsoft Visual Studio 2013 and Microsoft Visual Studio 2019.

Building with Visual Studio 201x

Double-click on the 2013 solution file **LivePlot.sln**
Retarget for later version if necessary
Change configuration to **Release**
Set platform to either **Win32** or **x64**
Select BUILD -> Build Solution

Building with Visual Studio 6

Descend into **LivePlot_v12\LivePlot** subfolder
Double-click on Workspace file **LivePlot.dsw**
Change configuration to **Win32 Release**
Select Build -> Build LivePlot.exe
Change last line of **LivePlot32.cmd** to **start Release\LivePlot.exe**

http://www.aholme.co.uk/PhaseNoise/Main.htm

Setting PATH and XILINX environment variables

LivePlot has two external dependencies which need to be on the PATH:

- FFTW **libfftw3-3.dll**
- Xilinx **libCseJtag.dll** Platform USB JTAG driver, the location of which changes with product (ISE or Lab Tools) and version (14.x or 13.x) installed.

The Xilinx JTAG driver needs the XILINX environment variable and will abruptly terminate the process if it is missing or set incorrectly!

```
ISE 14.7 64-bit
XILINX = C:\Xilinx\14.7\ISE_DS\ISE
PATH   = C:\Xilinx\14.7\ISE_DS\ISE\lib\nt64;..\fftw
ISE 14.7 32-bit
XILINX = C:\Xilinx\14.7\ISE_DS\ISE
PATH   = C:\Xilinx\14.7\ISE_DS\ISE\lib\nt;..\fftw
Lab Tools 14.7 32-bit
XILINX = C:\Xilinx\14.7\LabTools\LabTools
PATH   = C:\Xilinx\14.7\LabTools\LabTools\lib\nt;..\fftw
```

LivePlot32.cmd and **LivePlot64.cmd** launch scripts, and Visual Studio 201x **LivePlot.vcxproj.user** project settings (Configuration properties -> Debugging -> Environment) are configured as shown above for ISE 14.7 and need editing for a different version or install location.

Network settings and Windows Firewall

To receive packets from the SP605, LivePlot must be configured with the IP and MAC address of the Ethernet port. The MAC address field is populated automatically when a local IP address is selected from the drop down list in the Settings dialog.

Windows may treat the wired Ethernet port as either a public or a private network. When data capture is started for the first time, Windows Firewall asks permission to unblock LivePlot.exe, but the checkbox for public networks is not ticked by default.

If the Firewall dialog is cancelled or dismissed without ticking the public network box, open Windows Firewall in the Control Panel, find LivePlot.exe and grant permission there.

Windows 10 workaround

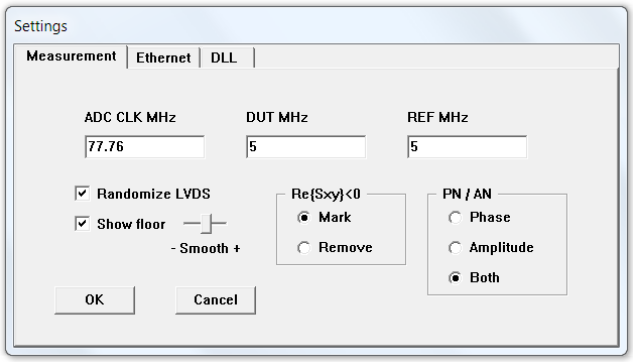
This involves using the 32-bit version of LivePlot through the 64-bit version of Xilinx **cse_server**:

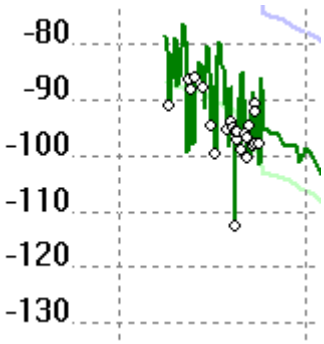
- Install October 2013 version of Xilinx ISE 14.7 (not the new Windows 10 version)
- Build 32-bit LivePlot
- Download and install 32-bit FFTW
- Create desktop shortcut to: C:\Xilinx\14.7\ISE_DS\ISE\bin\nt64\cse_server.exe
- Launch cse_server
- On DLL tab of the LivePlot settings dialog: change JTAG driver from libCseJtag.dll to libCseJtagClient.dll

What's new in LivePlot version 12?

- Amplitude noise (AN) and/or phase noise (PN) measurement
- Remove or mark invalid cross-correlation points where Re{Sxy}<0
- Smoothing of Im{Sxy} noise floor trace
- Supports LTC2175 LVDS randomizer (noise spreading)
- Late-binding to FFTW and Xilinx DLLs
- Windows 10 workaround

Settings dialog – Measurement tab





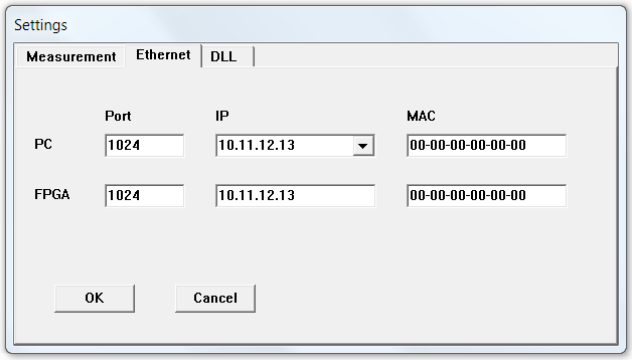
Randomize LVDS – turns on LVDS randomization to potentially reduce tones caused by interference from serial data outputs reaching ADC inputs. See "Digital output randomizer" LTC2175 datasheet page 24.

Show floor – display imaginary part of correlation cross product Im{Sxy} on real-time view. This gives an estimate of the system noise floor. The **Smooth** slider adjusts the strength of a moving average filter applied to the Im{Sxy} noise floor trace.

Re{Sxy}<0 – choose whether to mark or remove invalid data points where real part of correlation cross product is negative.

PN / AN – choose required measurement(s). Running both doubles network traffic.

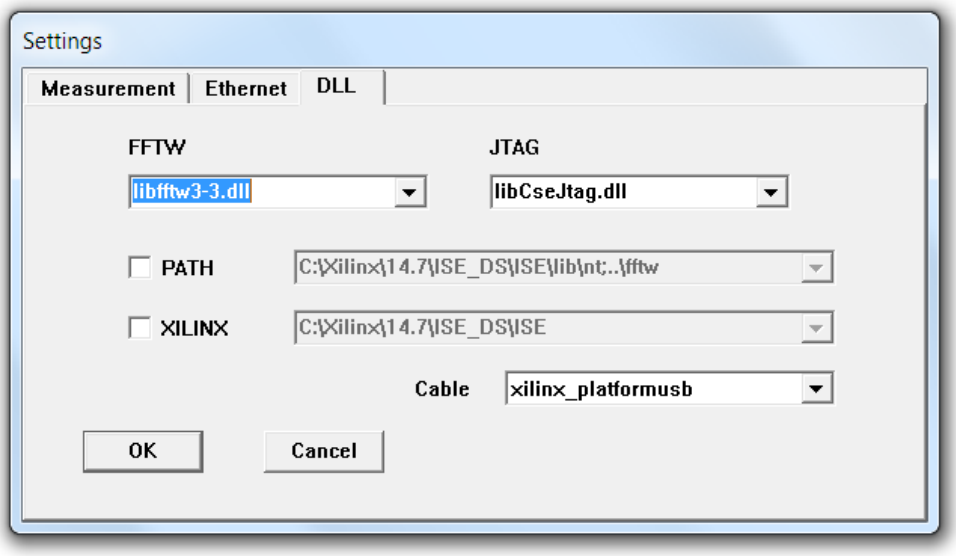
Settings dialog – Ethernet tab



Select local IP address from drop-down list of PC Ethernet port to which SP605 is connected. MAC address is automatically populated. Other fields can probably be left as default.

http://www.aholme.co.uk/PhaseNoise/Main.htm

Settings dialog – DLL tab



This is where it can get complicated, but most times the fields on this tab can be left at their default settings.

The **FFTW** field can be a path to the DLL, or just the DLL name (as shown above) in which case the PATH is searched to find it.

For Windows 10, select libCseJtagClient.dll from the drop-down on the **JTAG** field. Choose libCseJtag.dll on all other operating systems.

The **cable** should always be xilinx_platformusb

The **PATH** and **XILINX** environment variables must be set correctly to load the Xilinx JTAG driver DLLs. There are now four places where these variables can be set:

1. As global Windows environment variables in System Settings
2. Visual Studio project settings (Debugger -> Environment)
3. In a .cmd launcher script (e.g. LivePlot64.cmd)
4. Here, on the DLL tab of the Settings dialog

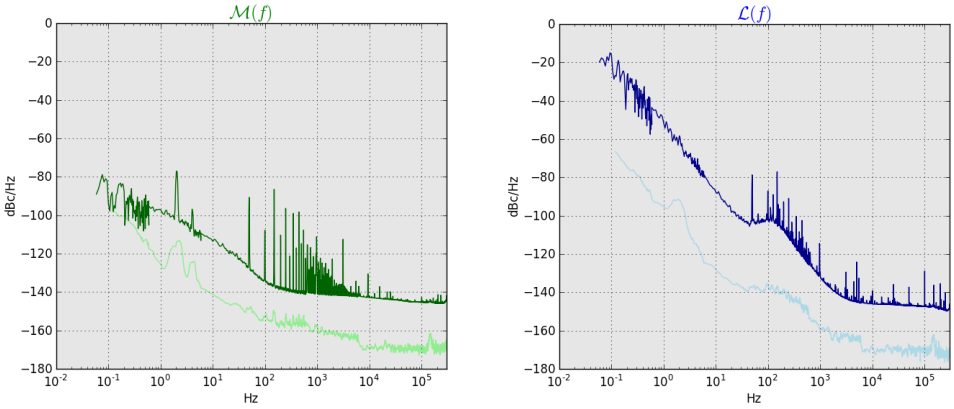
If the check boxes are not ticked, the **PATH** and **XILINX** environment variables used by LivePlot are those inherited from Windows or the parent process. Ticking a check box allows an alternative PATH or XILINX environment string to be entered. This does not change the global Windows environment, it only applies to LivePlot.

LivePlot now late-binds to the DLLs, meaning it delays loading them until it needs to communicate with the FPGA. The Xilinx JTAG driver will abruptly terminate the process at that point, if XILINX is set incorrectly.

If LivePlot cannot find a DLL, either because the name was entered incorrectly, or it was not found on the search PATH, LivePlot will display an error message.

Spectra.csv
Spectra.py
SpectraAN.png
SpectraPN.png

At the end of a measurement, LivePlot writes the data to Spectra.csv, which can be converted to graphs like those below using Python script Spectra.py or opened using Microsoft Excel or other software.



The output file name was changed to differentiate it from the old name (freq.txt) because the inclusion of both amplitude and phase data meant the format had to change. Columns in the CSV file are:

Hz	Offset from carrier
p.Re	log(abs(avg(Re{Sxy}))) phase noise
p.Im	log(abs(avg(Im{Sxy}))) phase noise
p<0	1 means illegitimate data point i.e. avg(Re{Sxy})<0
a.Re	log(abs(avg(Re{Sxy}))) amplitude noise
a.Im	log(abs(avg(Im{Sxy}))) amplitude noise
a<0	1 means illegitimate data point i.e. avg(Re{Sxy})<0
ADC	CLK frequency (Hz)
DUT	DUT frequency (Hz)
REF	REF frequency (Hz)
Samples	Total samples after decimation by 128 in FPGA

Runtime in seconds = 128 * Samples / ADC_CLK

The Python script applies a moving average filter to smooth noise floor data in the imaginary part. The works independently of any smoothing set in the GUI. The Python script removes illegitimate data points. This also works independently of the GUI setting.

Folder organisation

LivePlot is delivered as a Visual Studio project; however, it is not necessary to keep this folder structure once the executable has been built. LivePlot.exe, QuadChannel_v8.xsvf and libfftw3-3.dll are the only files required to do measurements. PATH setting can be simpler if libfftw3-3.dll and LivePlot.exe are in the same folder. There is no need to use .cmd scripts to launch the software. The PATH to the Xilinx bin folder can be setup via the settings dialog DLL tab.

Troubleshooting

LivePlot window suddenly vanishes on attempting to access hardware	Check XILINX environment variable setting on DLL tab
No error message; but no data appears after selecting Start	Check Windows Firewall permissions for LivePlot.exe on both public and private networks
"FPGA version mismatch or FPGA not loaded"	Remedy: select “Load FPGA” from system menu
"JTAG error"	Check USB JTAG cable connection
"Missing XSVF file"	Check if QuadChannel_v8.xsvf is on the PATH
"bind failed"	Ethernet problem. Check network cable and network settings.
"Error loading JTAG DLL"	Check PATH and name of Xilinx JTAG DLL on settings DLL tab
"Error loading FFTW"	Check PATH and name of FFTW DLL on settings DLL tab. Could also be 32 / 64 bit mismatch.
"Missed %d packet(s)"	UDP packets were dropped or arrived out of sequence. Try direct cable connection instead of working via switch / router. Disable Wi-Fi. Do not run CPU or network intensive software whilst making measurements. Update to latest version of NIC driver.
"WSAStartup failed" "Create socket failed" "setsockopt SO_RCVBUF failed" "WSAAsyncSelect failed"	Winsock errors
"recv() returned %d"	Check UDP port number
"Invalid XSVF file"	Check QuadChannel_v8.xsvf